Case No.: DENSE-049A

THERMAL RING USED IN 3-D STACKING

CROSS-REFERENCE TO RELATED APPLICATIONS

(Not Applicable)

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

(Not Applicable)

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to a heat dissipation structure for integrated circuit (IC) chip stacks, and more particularly to a thermal ring interposed in a 3-D chip stack.

[0002] As is currently known in the art, packaged components are often stacked using a variety of approaches. In all of the approaches to date, the concept has been to mount the stacks on the surface of a solid board such as a printed circuit board (PCB). More particularly, one of the most commonly used techniques to increase memory capacity is the stacking of memory devices into a vertical chip stack, sometimes referred to as 3D packaging or Z-Stacking. In the Z-Stacking process, from two to as many as eight memory devices or other integrated circuit (IC) chips are interconnected in a single component (i.e., a chip stack) which is mountable to the "footprint" typically used for a single packaged device such as a packaged chip. The Z-Stacking process has been found to be volumetrically efficient, with packaged chips in TSOP (thin small outline package) or LCC (leadless chip carrier) form generally

being considered to be the easiest to use. Some have used bare dies in the Z-Stacking process, however, such use tends to make the stacking process more complex and not well suited to automation.

[0003] As the components are stacked inside of the 3-D stack, it is difficult to obtain an effective and direct path for dissipating the heat generated thereby. This situation is more problematic for the 3-D stack incorporating high power electronic components with high heat dissipation ratings. Hence, there is an urgent need for thermal management to efficiently remove the heat from the 3-D stacks. The thermal performance of 3-D stacks is further challenging with the development of high-performance components, smaller packages and lower silicon operating temperatures.

BRIEF SUMMARY OF THE INVENTION

[0004] In accordance with the present invention, there is provided a chip stack comprising at least two carrier layers (i.e., an upper carrier layer and a lower carrier layer). Each of the carrier layers includes a first conductive pattern disposed thereon. The chip stack further comprises at least one thermal ring having a second conductive pattern disposed thereon. The thermal ring is disposed between the upper and lower carrier layers, with the second conductive pattern being electrically connected to the first conductive pattern of each of the carrier layers. In addition to the carrier layers and thermal ring, the chip stack comprises at least two integrated circuit chips which are electrically connected to respective ones of the first conductive patterns. The integrated circuit chip electrically connected to the first conductive pattern of the lower carrier layer is at least partially circumvented by the thermal ring and at least

partially covered by the upper carrier layer. The chip stack may further comprise a transposer layer having a third conductive pattern disposed thereon. If the transposer layer is included in the chip stack, the first conductive pattern of the lower carrier layer is electrically connected to the third conductive pattern of the transposer layer.

[0005] In the present chip stack, the thermal ring is formed to define a plurality of castellations. Defined between each adjacent pair of the castellations is a flow channel. The flow channels are operative to facilitate the circulation of air over the integrated circuit chip which is circumvented by the thermal ring and disposed between the carrier layers. To further assist in the heat dissipation function, a heat sink may be attached to the integrated circuit chip disposed between the carrier layers. Within each castellation of the thermal ring is one or more vias or feed-through holes which form a Z-axis interconnect. Once the thermal ring has been placed about the integrated circuit chip and between the carrier layers, the Z-axis connection is made from the thermal ring to the carrier layers. As indicated above, once the chip stack has been completely assembled, air is free to flow through the flow channels defined between the castellations in the thermal ring to cool the component(s) and the chip stack itself. The transposer layer of the chip stack translates the chip stack to route the I/O's of the integrated circuit devices to the appropriate pattern. The stacking approach of the present invention enables the stacking of the integrated circuit devices, one on top of the other, with vertical as well as horizontal interconnections. The configuration of the thermal ring addresses the thermal challenge of three-dimensional stacks by providing the cooling function described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] These as well as other features of the present invention will become more apparent upon reference to the drawings wherein:

[0007] Figure 1 is a top perspective view of a chip stack including a thermal ring constructed in accordance with the present invention;

[0008] Figure 2 is an exploded view of the chip stack shown in Figure 1; and

[0009] Figure 3 is a top perspective view of the thermal ring shown in Figures 1 and 2.

DETAILED DESCRIPTION OF THE INVENTION

[0010] Referring now to the drawings wherein the showings are for purposes of illustrating a preferred embodiment of the present invention only, and not for purposes of limiting the same, Figure 1 perspectively illustrates a chip stack 10 constructed in accordance with the present invention. The chip stack 10 comprises at least two identically configured component carrier layers 12. Each of the component carrier layers 12 is rectangularly configured and defines opposed, generally planar top and bottom surfaces, an opposed pair of longitudinal peripheral edge segments, and an opposed pair of lateral peripheral edge segments.

[0011] Disposed on each component carrier layer 12 is a first conductive pad array which itself preferably comprises a first set of carrier pads 14 and a second set of carrier pads 16. The carrier pads 14 of the first set are preferably arranged in a generally rectangular pattern or array in the central portion of the top surface of each carrier layer 12. The carrier pads 16 of the second set are preferably arranged so as to extend linearly along the

longitudinal and lateral peripheral edge segments of each carrier layer 12. The carrier pads 14 of the first set are electrically connected to respective ones of the carrier pads 16 of the second set via conductive traces 17.

[0012] In addition to the carrier pads 14, 16 of the first and second sets, the first conductive pad array of each carrier layer 12 comprises a third set of carrier pads which are disposed on the bottom surface of the carrier layer 12. The carrier pads of the third set are preferably arranged in an identical pattern to the carrier pads 16 of the second set, and extend linearly along the longitudinal and lateral peripheral edge segments of the carrier layer 12 such that each of the carrier pads of the third set is aligned with and electrically connected to a respective one of the carrier pads 16 of the second set. Such electrical connection is preferably facilitated through the use of a via or feed-through hole.

[0013] In addition to the carrier layers 12, the chip stack 10 of the present invention comprises at least one rectangularly configured interposer thermal ring 18. The thermal ring 18 defines opposed top and bottom surfaces, an opposed pair of longitudinal side sections, and an opposed pair of lateral side sections. Disposed on the thermal ring 18 is a second conductive pad array which itself preferably comprises a first set of ring pads 20 disposed on the top surface, and a second set of ring pads disposed on the bottom surface. The ring pads 20 of the first set and ring pads of the second set are preferably arranged in patterns which are identical to each other, and to the patterns of the carrier pads 16 of the second set and carrier pads of the third set of each of the carrier layers 12. In this respect, the ring pads 20 of the first set and ring pads of the second set each extend linearly along the longitudinal and lateral side sections of the thermal ring

18, with each of the ring pads 20 of the first set being aligned with and electrically connected to a respective one of the ring pads of the second set. Similar to the electrical connection of the carrier pads 16 of the second set to the carrier pads of the third set, the electrical connection of each of the ring pads 20 of the first set to a respective one of the ring pads of the second set may be accomplished through the use of a via or feed-through hole.

[0014] As best seen in Figure 3, the longitudinal side sections of the thermal ring 18 are each preferably crenellated so as to define a series of castellations 22. Each adjacent pair of castellations 22 is separated by a rectangularly configured flow channel 24, with each of the outermost pair of castellations 22 of each longitudinal side section being separated from the remainder of the thermal ring 18 by a flow channel 24. The castellations 22 and flow channels 24 are formed within each of the longitudinal side sections of the thermal ring 18. The flow channels 24 extend downwardly from the top surface of the thermal ring 18 to a depth equal to approximately half of the total thickness or height thereof. Additionally, as seen in Figures 2 and 3, the ring pads 20 of the first set are arranged such that a pair of ring pads 20 are included upon each of the castellations 22.

[0015] Those of ordinary skill in the art will recognize that different numbers of castellations 22 and flow channels 24 may be included in each of the longitudinal side sections of the thermal ring 18, and that such castellations 22 and flow channels 24 may be formed in the lateral side sections of the thermal ring 18 as well. Moreover, the depth and cross-sectional configuration of each of the flow channels 24 may be varied. The thermal ring 18 is preferably fabricated from a printed circuit board (PCB) substrate material or other thermally managed

material. The vias extending between corresponding pairs of the ring pads 20 of the first set and the ring pads of the second set provide a Z-axis interconnect, as do the vias extending between corresponding pairs of the carrier pads 16 of the second set and carrier pads of the third set in each of the carrier layers 12. As will be discussed in more detail below, the flow channels 24 provide air flow passages from the exterior of the thermal ring 18 into a rectangularly configured opening 26 defined thereby.

[0016] In the chip stack 10, the thermal ring 18 is disposed between the carrier layers 12, with the second conductive pattern of the thermal ring 18 being electrically connected to the first conductive pattern of each of the carrier layers 12. More particularly, the ring pads of the second set are electrically connected to respective ones of the carrier pads 16 of the second set of one of the carrier layers 12 (i.e., the carrier layer 12 immediately below the thermal ring 18 in the chip stack 10), with the ring pads 20 of the first set being electrically connected to respective ones of the carrier pads of the third set of one of the carrier layers 12 (i.e., the carrier layer 12 immediately above the thermal ring 18 in the chip stack 10). Due to the carrier pads 16 of the second set, carrier pads of the third set, ring pads 20 of the first set, and ring pads of the second set all being arranged in identical patterns, each coaxially aligned pair of ring pads is itself coaxially aligned with a coaxially aligned set of carrier pads of the second and third sets of each of the adjacent carrier layers 12. The electrical connection of the second conductive pattern of the thermal ring 18 to the first conductive pattern of each of the adjacent carrier layers 12 is preferably facilitated via a soldering process.

[0017] Referring now to Figures 1 and 2, the chip stack

10 of the present invention may further comprise a rectangularly configured transposer layer 28 which defines opposed, generally planar top and bottom surfaces, an opposed pair of longitudinal peripheral edge segments, and an opposed pair of lateral peripheral edge segments. Disposed on the transposer layer 28 is a third conductive pattern. The third conductive pattern comprises a first set of transposer pads 30 which are disposed on the top surface of the transposer layer 28, and a second set of transposer pads which are disposed on the bottom surface thereof. The transposer pads 30 of the first set are electrically connected to respective ones of the transposer pads of the second set. The transposer pads 30 of the first set are preferably arranged in a pattern which is identical to the patterns of the second set of carrier pads 16, third set of carrier pads, first set of ring pads 20 and second set of ring pads. In this respect, the transposer pads 30 of the first set extend linearly along the longitudinal and lateral peripheral edge segments of the transposer layer 28. The transposer pads of the second set may be arranged in any pattern as required to electrically interface the chip stack 10 to a desired footprint on a printed circuit board or other substrate. The pattern of the transposer pads of the second set may be identical to that of the carrier pads 14 of the first set so as to mimic a BGA pattern.

[0018] If the transposer layer 28 is included in the chip stack 10, the first conductive pattern of one of the carrier layers 12 (i.e., the lowermost carrier layer 12 in the chip stack 10) is electrically connected to the third conductive pattern of the transposer layer 28. More particularly, each of the carrier pads of the third set of the lowermost carrier layer 12 is electrically connected to a respective one of the transposer pads 30 of the first

set. Due to the carrier pads of the third set and the transposer pads 30 of the first set being arranged in identical patterns, each of the carrier pads of the third set is coaxially alignable with a respective one of the transposer pads 30 of the first set, with the electrical connection therebetween preferably being facilitated via soldering. The transposer layer 28 and carrier layers 12, like the thermal ring 18, are also preferably fabricated from a printed circuit board material or other material having thermal dissipation properties.

[0019] As best seen in Figure 2, the chip stack 10 of the present invention further comprises at least two identically configured integrated circuit chips, and more particularly packaged chips 32, which are electrically connected to respective ones of the first conductive patterns of the carrier layers 12. Each of the packaged chips 32 comprises a rectangularly configured body 34 defining opposed, generally planar top and bottom surfaces, an opposed pair of longitudinal sides, and an opposed pair of lateral sides. Disposed on the bottom surface of the body 34 are a plurality of conductive contacts which are arranged in a pattern identical to that of the carrier pads 14 of the first set of each of the carrier layers 12. The conductive contacts of each of the packaged chips 32 are electrically connected to respective ones of the carrier pads 14 of the first set of a respective one of the first conductive patterns of the carrier layers 12. Due to the conductive contacts of the packaged chips 32 and the carrier pads 14 of each of the first sets being arranged in identical patterns, the conductive contacts of each of the packaged chips 32 are coaxially alignable with respective ones of the carrier pads 14 of the corresponding first set. The electrical connection of the conductive contacts of each packaged chip 32 to respective ones of the carrier

pads 14 of the first set of a respective one of the first conductive patterns is preferably accomplished via soldering. Each of the packaged chips 32 may be a BGA (ball grid array) device, also referred to as a CSP (chip scale package), micro-BGA, or a flip chip. As indicated above, each of the packaged chips 32 has solder ball interconnects located in rows and columns on the bottom surface of the body 34.

[0020] The complete chip stack 10 shown in Figure 1 includes the transposer layer 28, two carrier layers 12, one thermal ring 18, and two packaged chips 32. The first conductive pattern of the lowermost carrier layer 12 is connected to the third conductive pattern of the transposer layer 28 in the above-described manner. Additionally, the thermal ring 18 is disposed or positioned between the carrier layers 12, with the second conductive pattern of the thermal ring 18 being electrically connected to the first conductive pattern of each of the carrier layers 12 in the above-described manner. Since the conductive contacts of each of the packaged chips 32 are electrically connected to respective ones of the carrier pads 14 of the first set of respective ones of the first conductive patterns, the lowermost packaged chip 32 within the chip stack 10 is disposed between the carrier layers 12 and circumvented by the thermal ring 18. Thus, such lowermost packaged chip 32 resides within the opening 26 defined by the thermal ring 18, with the body 34 of the packaged chip 32 and thermal ring 18 preferably being sized relative to each other such that the top surface of the body 34 does not protrude beyond the top surface of the thermal ring 18.

[0021] As indicated above, the various electrical connections within the chip stack 10 are preferably facilitated through the use of standard solder joints or through the use of alternative interconnect methods. Those

of ordinary skill in the art will recognize that the chip stack 10 may be formed to include more than two carrier layers 12, one thermal ring 18, and two packaged chips 32.

[0022] In the complete chip stack 10, the structural attributes of the thermal ring 18, and in particular the flow channels 24 formed therein, are used to provide air flow over and about the packaged chip 32 captured between the carrier layers 12 and circumvented by the thermal ring 18, thus effectively cooling the same. As seen in Figure 2, if the packaged chip 32 comprises an extremely high temperature component, thermal dissipation can be further increased by attaching a heat sink 36 to the top surface of the body 34 of any packaged chip(s) 32 circumvented by the thermal ring(s) 18. The heat sink 36 may be attached to the body 34 through the use of an adhesive, and is preferably fabricated from a thermally conductive material such as copper. As will be recognized, the inclusion of the heat sink 36 within the chip stack 10 allows heat to dissipate through the copper of the heat sink 36 and to be carried away by the air current flowing through the flow channels 24 defined between the castellations 22 within the thermal ring 18.

[0023] In forming the chip stack 10, the various layers can be easily stacked using a panel format, with the stacked panels then being separated using standard PCB routing procedures to form the chip stacks 10. For example, typical four inch by six inch panels with multiple stack sites may be processed, then stacked in a conventional stacking fixture. Such panels can easily be designed with multiple devices per layer for each chip stack 10. In this regard, multiple devices such as BGAs, TSOPs (thin small outline packages), or bare dies can be intermixed and placed on one carrier layer 12. Additionally, it is contemplated that the chip stack 10 may

be manufactured in a manner wherein the lowermost carrier layer 12 and transposer layer 28 may be combined into a single substrate or layer. As indicated above, though Figures 1-3 show the chip stack 10 as a two component stack, additional layers/devices can be assembled in the above-described manner.

[0024] Additional modifications and improvements of the present invention may also be apparent to those of ordinary skill in the art. Thus, the particular combination of parts described and illustrated herein is intended to represent only certain embodiments of the present invention, and is not intended to serve as limitations of alternative devices within the spirit and scope of the invention.